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**Question Paper Code : 61171**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Sixth/Seventh Semester

Electronics and Communication Engineering

CS 1358 — COMPUTER ARCHITECTURE

(Common to Electrical and Electronics Engineering, Electronics and Instrumentation Engineering, and Instrumentation Control Engineering)

(Regulation 2008)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate Embedded Computer and Personal Computer.
2. Differentiate between big-endian and Little -endian
3. Compare Ripple carry adder and carry look ahead adder.
4. Write the Basic IEEE format for Floating point.
5. Define instruction pipelining.
6. What is data hazards?
7. Define memory latency.
8. How to estimate the improvement in the memory performance from using cache?
9. What is bus arbitration?
10. Define SCSI Bus.

PART B — (5 × 16 = 80 marks)

11. (a) (i) What will be the content of PC and memory, while executing a branch instruction? Give example. (8)
- (ii) Which addressing mode is suitable for dealing lists and arrays? List out various addressing modes with example. (8)

Or

- (b) (i) What is the difference between the stack and queue? How the data operated by a program are stored in stack? (8)
- (ii) Which method is suitable and simple to read a character through keyboard for display? What are the limitations of that method? (8)
12. (a) (i) Design a carry look ahead adder for 4 bit and analyze the carry propagation method. (10)
- (ii) Write the IEEE standard for double precision and single precision. (6)

Or

- (b) (i) How the multiplication is simplified by carry save adder? Give example. (8)
- (ii) Illustrate the floating point addition-subtraction unit. (8)
13. (a) (i) Draw the timing diagram of a memory read operation. (8)
- (ii) What are the advantages of multiple bus? Explain the three bus organization of the datapath. (8)

Or

- (b) (i) When the instruction Hazards will occur? Analyze the idle cycle caused by pipeline stall in branch instruction. (8)
- (ii) Differentiate pipeline operation and superscalar operation. Which approach is used to achieve superscalar processor? (8)
14. (a) How the bit cells are organized in a memory chip? Describe it. (16)

Or

- (b) (i) What is the need for virtual memory? What is the method used by the processor to generate virtual address? Describe it. (10)
- (ii) How the datas are stored in CD? (6)
15. (a) What are the different standard I/O interfaces available? Describe how the Peripherals are connected using PCI? Give the timing diagram for read operation on PCI bus. (16)

Or

- (b) (i) How DMA controller enables the data transfer from I/O devices? Explain it. (8)
- (ii) How bus arbitration can be handled by daisy chain? Explain it. (8)